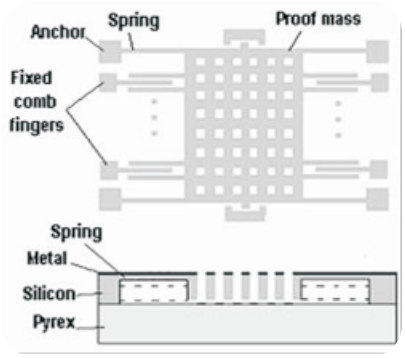
THE OPTIMISED CAPACITIVE INERTIAL SENSOR

A new design and fabrication process of silicon micromachined inertial capacitive sensor, with performance-to-cost improving is described. The inertial sensor structures were fabricated using silicon, anodic bonding to Pyrex glass and Deep Reactive Ion Etching (DRIE). The sensor sensitivity increases and the natural frequency of the system decreases by: increasing the mass of the sensor, increasing the length of the spring, decreasing the width of the spring, decreasing the thickness of the spring. In order to maintain the nonlinearity of the sensor in the range of 1%, the changing in capacitance should not exceed 10% of the capacitance at zero acceleration. The capacitance can be increase in three ways: increasing the dielectric constant (if it is possible), decreasing the space between the plates (there is a limit imposed by the fabrication) or increasing the surface area. The last solution can be very easy done with increasing of the thickness.

A schematic view of the test-design is presented in Fig. 1. A 100 μm thick silicon wafer is bonded on a Pyrex glass. The design was made for 80 pairs of combs and an inertial mass of $1x10^{-7}$kg. According with the acceleration range was to 1g, 2g and 5g; the thickness of the spring was 20μm, 40μm and 100μm.



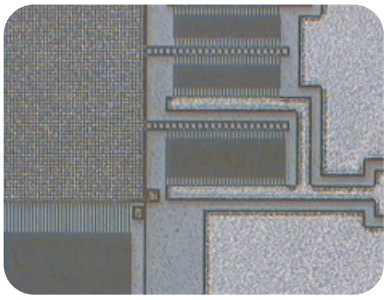


Fig.1. *Schematic view of the accelerometer design (left) and the photograph of the accelerometer structure*

FABRICATION PROCESS

The process starts with a photolithographic process made on the polish surface of silicon process using AZ7220 photoresist, with a thickness of 8 μm, process using a CEE spin-coater (3000rpm/30 sec) and a Karl Suss mask aligner. This mask was used for deep trench generated with STS ICP DRIE, SF_6/O_2 of 130 sccm/13 sccm gases were used for the etch cycle of 8 seconds with 800 W coil power and 130 W platen power, C_4F_8 was used for the passivation cycle of 5
seconds with 800 W coil power only. In the third step of fabrication process the silicon is wafer-to-wafer anodically bonded to the Pyrex glass (Corning 7740). The parameter of the bonding process was selected in order to minimize the bowing of the wafer. The Pyrex glass Corning 7740 seams to be the most suitable glass for such application. The silicon wafer was then thinned down to 100 μm using 30% KOH solution at 80°C. The thinned silicon wafer etched by KOH has good surface roughness of about 100 nm. The patterned wafer was baked at 1300C for 10 min. This photolithography process ensures a good patterning of 2 μm thick photoresist for the consequent DRIE etching of high aspect ratio silicon structures of 100 μm in thickness. The patterned silicon/glass wafer was etched using STS ICP DRIE system. The process parameter setting gives an etch rate of about 1.8 μm/min with almost vertically etched sidewalls of silicon structures. After 55 min, the etching has reached the bottom of silicon wafer and stopped on the glass substrate.

RESULTS AND DISCUSSIONS

At high plasma densities, the charge builds up at the surface of Pyrex glass due to its electrical isolation property when the DRIE etches the silicon trenches through the top silicon all the way to the glass. The further incoming ions repelling and are then deflected into the sidewalls of the silicon beams. This causes a high lateral etch rate at the silicon/glass interface. This effect is called notching effect and should be minimized for the normal MEMS applications using SOI wafers or silicon / Pyrex glass bonding. A successful and efficient way is to modify the RF source frequency from 13. 56 MHz to 380 kHz. By optimizing DRIE processing parameters, however, we use this notching effect to release the silicon microstructures from the bonded Pyrex glass. Fig. 2 presents the fixed combs released from the glass and a spring of an inertial sensor with high aspect ratio. In the silicon microstructure release process using the notching effect of DRIE, the released air gap to the glass substrate is very dependent on the width of silicon microstructures. Narrower silicon beams result in larger released air gap. In our study the silicon beams in comb drives is 3 μm and the holes distance in the proof mass is 10 μm. To release the proof mass from the glass substrate, longer over etching is needed, which results in the larger air gap of about 40 μm in the comb drives as shown in figure 3. Therefore if the same thickness of all released structures is required, one should design the MEMS devices with the same widths for all the silicon microstructures to be release using this one-mask process. One can also design the different widths for comb drives, proof mass and spring supporting beams of accelerometers as studied in this letter to optimize its sensitivity. Another advantage of the process is the fabrication of inertial sensors for different ranges, with the same mask only by adjusting the time of the process (first deep RIE etching). In the last step of metal deposition, an electron beam evaporation process was used instead of the sputtering because the metal should not deposit the sidewalls of the silicon. Furthermore, due to the over etched silicon at the interface to the glass substrate, the metal will be deposited only on the top silicon and the bottom glass between released silicon structures.

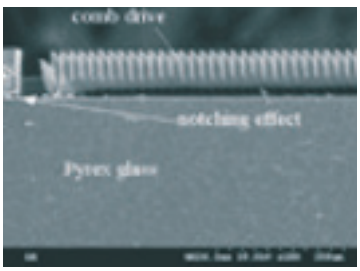


Figure 2 *SEM photograph of released silicon beams*

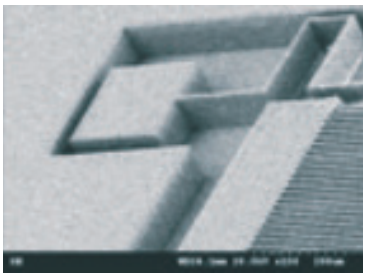


Figure 3 *SEM photograph of DRIE processed accelerometer*

CONCLUSIONS

A two-mask process technology is proposed to fabricate silicon capacitive inertial sensors using comb drive structures. A conductive silicon wafer is anodically bonded on Pyrex glass substrate. The high aspect ratio silicon inertial sensor structure was micromachined using DRIE and released from the glass substrate by further DRIE due to its notching effect. The spring stiffness was adjusted with another DRIE process. In this way, inertial sensors with different range can be process using same masks only by changing the spring stiffness.

Marioara Avram, Ciprian Iliescu[1], Andrei Marius Avram
National Institute for Research and Development in Microtechnologies, Bucharest, Romania,
[1]Institute of Bioengineering and Nanotechnologies- 51 Science Park Road, Singapore 117586